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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/076,625	02/19/2002	Atsushi Sakai	50006-138	9551

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EXAMINER	
ROSS, JOHN M	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 03/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/076,625	SAKAI ET AL.	
	Examiner	Art Unit	
	John M Ross	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 3, 5, 7, 9, 11, 17, and 19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5,7,9,11,17 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

1. Claims 1, 3, 5, 7, 9, 11, 17, and 19 are pending in the application.

Claims 1, 3, 5, 7, 9, 11, 17, and 19 are rejected.

Response to Amendment

2. Applicant's request for withdrawal of the finality of the rejection made in the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

3. Applicant's arguments filed on 11 February 2005 in response to the office action mailed on 12 November 2004 have been fully considered, but they are not persuasive. Therefore the rejections made in the previous office action are maintained and restated below.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3, 5, 9, 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiwara (Takashi Fujiwara et al, A Custom Processor for the Multiprocessor System

ASCA, 1998) in view of Hallnor (Erik G. Hallnor et al, A Fully Associative Software-Managed Cache Design, 2000).

As in claim 1, Fujiwara describes a cache memory system comprising:

a software cache controller which performs software control for controlling data transfer to the cache memory in accordance with a preliminarily programmed software (Fig.6; section 3.1.3, lines 1-10); and

a hardware cache controller which performs hardware control for controlling data transfer to the cache memory using a predetermined hardware (Section 3.1.3, lines 26-32);

wherein the processor causes the software cache controller to perform the software control but causes the hardware cache controller to perform the hardware control when it becomes impossible to perform the software control (Section 3.1.3, lines 32-36), and

where the processor automatically causes the hardware cache controller to perform hardware control when a cache miss happens at the time of software control (Section 3.1.3, lines 32-36).

Fujiwara does not teach that the hardware cache controller performs line management of the cache memory by using a multi-way set-associative method and that the software cache controller performs line management of the cache memory by using a fully-associative method for at least one way in the multiple ways, as required by claim 1.

It was well known to those of ordinary skill in the art at the time of invention by applicant that a cache line management policy may be multi-way set-associative or fully-associative. Hallnor teaches that hardware controlled management is better suited for a low-associativity cache (i.e. multi-way set-associative) due to the reduced complexity compared to a fully-associative cache, and software controlled management is better for fully-associative caches due to the ability to apply sophisticated replacement algorithms (Section 2, paragraphs 1, 3 and 4).

Regarding claim 1, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to perform hardware controlled line management of the cache memory by using a multi-way set-associative method, and to perform software controlled line management of the cache memory by using a fully-associative method as taught by Hallnor, in the system of Fujiwara, according to the teaching of Hallnor that the reduced complexity of a multi-way set-associative cache is better suited to hardware control, and to take advantage of the ability to apply sophisticated replacement algorithms to a software-managed fully-associative cache.

As in claims 3, Fujiwara describes the above system wherein the software cache controller stores desired data in the cache memory in accordance with a code produced by static prediction of a compiler (Section 3.1.3, lines 8-10).

As in claim 5, Fujiwara describes the above system wherein before the processor executes a data read-out instruction for reading out desired data of the main memory, the

software cache controller reads out data at an address of the main memory designated by the data read-out instruction and stores the data in the cache memory (Section 3.1.3, lines 12-13).

As in claim 9, Fujiwara describes the above system wherein before the processor executes a data write instruction for writing data in the main memory, the software cache controller designates an address of the cache memory, which is used for storing data from the processor (Section 3.1.3, lines 12-13).

As in claims 17 and 20, Fujiwara describes the above system wherein the software cache controller is formed by a transfer control processor for controlling data transfer to the cache memory (Fig. 6, element labeled "Data Transfer Controller"; section 3.1.3, lines 6-8).

6. Claims 7 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujiwara (Takashi Fujiwara et al, A Custom Processor for the Multiprocessor System ASCA, 1998) in view of Hallnor (Erik G. Hallnor et al, A Fully Associative Software-Managed Cache Design, 2000) as applied to claims 5 and 9 above, and further in view of Handy (Jim Handy, The Cache Memory Book, 1998).

Fujiwara is relied upon for the teachings relative to claims 5 and 9 as above.

Fujiwara does not teach that at the same time when the processor executes a data read-out instruction, the software cache controller transfers from the cache memory to the processor the

data at the address of the main memory designated by the data read-out instruction, as required by claim 7.

Fujiwara also does not teach that when the processor executes a data write instruction, the data from the processor written at the designated address of the cache memory is written by the software cache controller at an address of the main memory designated by the data write instruction, as require by claim 11.

It is noted that claim 7 describes a cache read hit, and claim 11 describes a cache write hit with a write-through policy. Handy teaches that during a cache read hit a cache controller transfers data from the cache memory to the processor (Fig. 2.4a; page 44, paragraph 1). Handy also teaches that during a cache write hit, the cache controller writes data in the cache memory and the main memory (Fig. 2.4c; page 45, paragraph 3). Handy also teaches that using a cache memory greatly increases effective memory speed (Page 204, paragraph 10).

Regarding claims 7 and 11, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to transfer data from the cache memory to the processor during a cache read hit and to write data in the cache memory and the main memory during a cache write hit as taught by Handy, in the system of Fujiwara, in order to increase effective memory speed through the use of a cache memory as taught by Handy.

Response to Arguments

7. Applicant's arguments filed 11 February 2005 with respect to the rejection of claim 1 have been fully considered but they are not persuasive.

Applicant argues that the Hallnor reference ***"does not suggest hardware management by using a set-associative method for multiple ways and the software management by using a fully associative method for at least one way in the multiple ways"*** (Page 4).

In response to applicant's arguments, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. Rather, the test for obviousness is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

As noted in the prior office action and restated above, Fujiwara is relied upon for the teaching of a cache alternately managed by hardware and software. Fujiwara is silent as to the management policies of the cache.

Examiner previously noted and has restated above that multi-way set associative and fully-associative cache management policies were well known at the time of invention by applicant. As evidence of this fact please see pages 51-54 of The Cache Memory Book by Jim Handy, which have been provided with this office action.

What is needed is a motivation to apply either of these well-known policies to the hardware and software cache management of Fujiwara. Hallnor provides this motivation as stated previously and restated in the rejection above. In short, Hallnor teaches that hardware control is best suited to a low-associativity management policy, and software control is better for a fully-associative management policy.

Noting that a multi-way set-associative cache is also a low-associativity cache, one of ordinary skill would therefore be motivated by Hallnor's teaching to apply this well-known type of cache management policy to the case of hardware control in Fujiwara. Similarly, Hallnor's teaching would suggest applying a fully-associative cache management policy to the case of software control in Fujiwara. Furthermore because the cache is the same physical cache under both management policies, the fully-associative cache management implemented by software control would necessarily operate on at least one of the multiple ways managed by the hardware.

Applicant further asserts that because Hallnor teaches advantages of using software management over hardware management, Hallnor therefore teaches away from a combined hardware and software cache controller (Page 5).

Examiner is not persuaded. Fujiwara is relied upon for the teaching of a combined hardware and software cache controller as stated in the rejection above. Hallnor's teaching related to advantages of software control over hardware control cannot eclipse the explicit teachings set forth by Fujiwara. In fact, Fujiwara was well aware of such advantages when stating that "a large software cache ... excludes the uncertain factor ... of the hardware cache"

(Fujiwara, § 3.1.3, lines 1-3). However, Fujiwara also recognizes limitations intrinsic to a software cache that lead to a solution involving the combining of hardware and software cache control (Fujiwara, § 3.1.3, lines 26-36).

Applicant argues that examiner has not given adequate consideration to the particular problems and solutions addressed by the claimed invention, then outlines particular problems associated with switching between software and hardware cache control, and asserts that claim 1 as recited provides a solution to these problems while the applied references do not (Pages 5-6).

In response, examiner contends that the combination of references cited in the rejection of claim 1 answers each limitation as set forth in the claim. The limitations corresponding to the particular problem set forth by applicant on page 6 do not appear in the claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Furthermore, the reason or motivation to modify a reference may often suggest what the inventor has done, but for a different purpose or to solve a different problem. It is not necessary that the prior art suggest the combination to achieve the same advantage or result discovered by applicant. See *In re Linter*, 458 F.2d 1013, 173 USPQ 560 (CCPA 1972); *In re Dillon*, 919 F.2d 688, 16 USPQ2d 1897 (Fed. Cir. 1990).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John M Ross whose telephone number is (571) 272-4212. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JMR

2/25/05

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER